

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Original) A method of manufacturing an integrated circuit having trench
2 isolation regions in a substrate including a first layer, the method comprising:
3 selectively etching the first layer to form apertures associated with locations of
4 the trench isolation regions;
5 forming strained semiconductor material above the first layer; and
6 forming insulative material in the apertures to form the trench isolation
7 regions.
- 1 2. (Original) The method of claim 1, wherein the strained semiconductor
2 material is formed on sidewalls of the apertures.
- 1 3. (Withdrawn) The method of claim 1, wherein strained semiconductor material
2 is formed after the insulative material is formed.
- 1 4. (Original) The method of claim 1, wherein the strained semiconductor
2 material is formed before the insulative material is formed.
- 1 5. (Withdrawn) The method of claim 3, wherein the strained semiconductor
2 material is formed by selective epitaxial growth.
- 1 6. (Original) The method of claim 1, further comprising:
2 siliciding the strained semiconductor material.
- 1 7. (Original) The method of claim 1, wherein the strained semiconductor
2 material is silicon and the first layer is silicon-germanium.
- 1 8. (Original) The method of claim 1, wherein the first layer is above a BOX
2 layer.

1 9. (Original) A method of forming shallow trench isolation structures in a
2 compound semiconductor layer above a buried oxide (BOX) layer, the method comprising:
3 providing a hard mask layer above the compound semiconductor layer;
4 removing the hard mask layer at locations;
5 forming trenches in the compound semiconductor layer under the locations;
6 stripping the hard mask layer;
7 forming a strained semiconductor layer above the compound semiconductor
8 layer; and
9 providing isolation material in the trenches to form the shallow trench
10 isolation structures.

1 10. (Original) The method of claim 9, further comprising providing a silicide
2 layer above the strained semiconductor layer.

1 11. (Withdrawn) The method of claim 10, wherein the strained semiconductor
2 layer is provided by selective silicon epitaxial growth.

1 12. (Original) The method of claim 9, wherein the isolation material is provided
2 by deposition.

1 13. (Original) The method of claim 12, further comprising providing a liner in the
2 trenches at low temperature.

1 14. (Original) The method of claim 13, wherein the low temperature is below
2 750°C.

1 15. (Original) The method of claim 14, wherein the liner is silicon dioxide grown
2 in an oxygen-containing atmosphere.

1 16. (Original) The method of claim 9, wherein the trenches have a bottom
2 reaching the BOX layer.

1 17. (Cancelled) An integrated circuit, comprising:
2 a compound semiconductor layer;
3 a buried oxide (BOX) layer beneath the compound semiconductor layer;
4 a strained semiconductor layer above the compound semiconductor layer; and
5 isolation trenches disposed in the compound semiconductor layer, wherein the
6 isolation trenches include insulative material and sidewalls, the sidewalls of the isolation
7 trenches are at least partially covered by the strained semiconductor layer.

1 18. (Cancelled) The integrated circuit of claim 17, further comprising a gate
2 structure between the isolation trenches.

1 19. (Cancelled) The integrated circuit of claim 18, wherein the strained
2 semiconductor layer is silicided at a location of a source and a drain.

1 20. (Cancelled) The integrated circuit of claim 17, wherein the strained
2 semiconductor material is silicon and the compound semiconductor material is silicon-
3 germanium and the trenches extend from the strained semiconductor material at a top to the
4 buried oxide layer at a bottom.

1 21. (New) A method for producing an integrated circuit, comprising:
2 providing a buried oxide (BOX) layer;
3 providing a compound semiconductor layer above the BOX layer;
4 providing a strained semiconductor layer above the compound semiconductor
5 layer; and
6 providing isolation trenches disposed in the compound semiconductor layer,
7 wherein the isolation trenches include insulative material and sidewalls, the sidewalls of the
8 isolation trenches are at least partially covered by the strained semiconductor layer.

1 22. (New) The method of claim 21, further comprising providing a gate structure
2 between the isolation trenches.

1 23. (New) The method of claim 22, further comprising siliciding the strained
2 semiconductor layer at a location of a source and a drain.

1 24. (New) The method of claim 21, wherein the strained semiconductor material
2 is silicon and the compound semiconductor material is silicon-germanium and the trenches
3 extend from the strained semiconductor material at a top to the buried oxide layer at a bottom.